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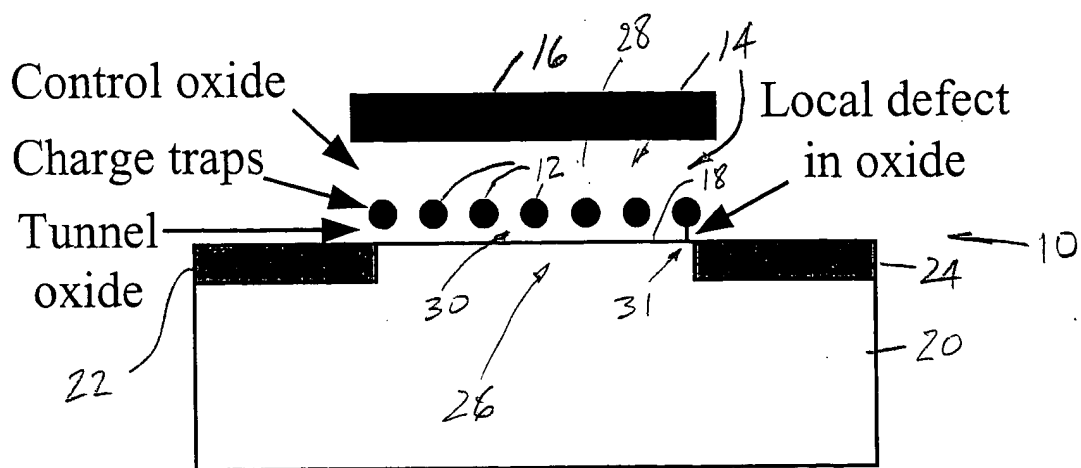


FIG. 1(a)

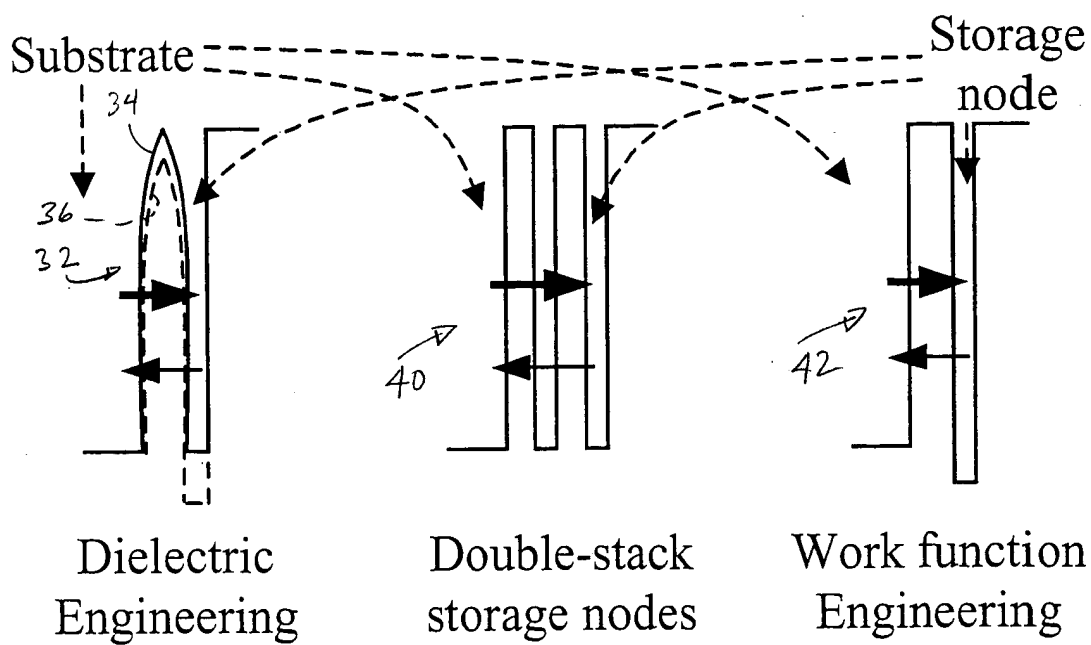


FIG 1(b)

(b)  
FIG 1(c)

FIG 1(d)

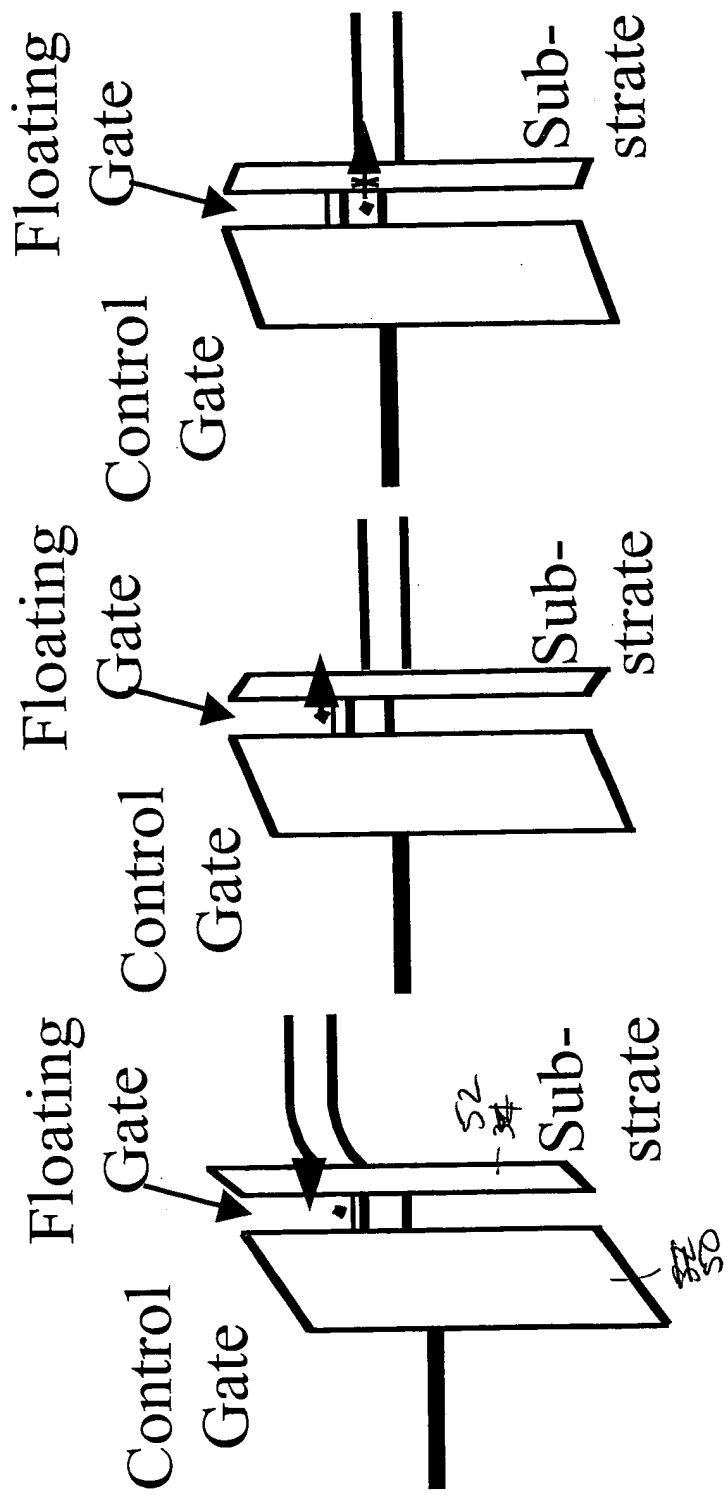


FIG. 2(a)  
(writing)

FIG. 2(b)  
(retention)

FIG. 2(c)  
(retention)

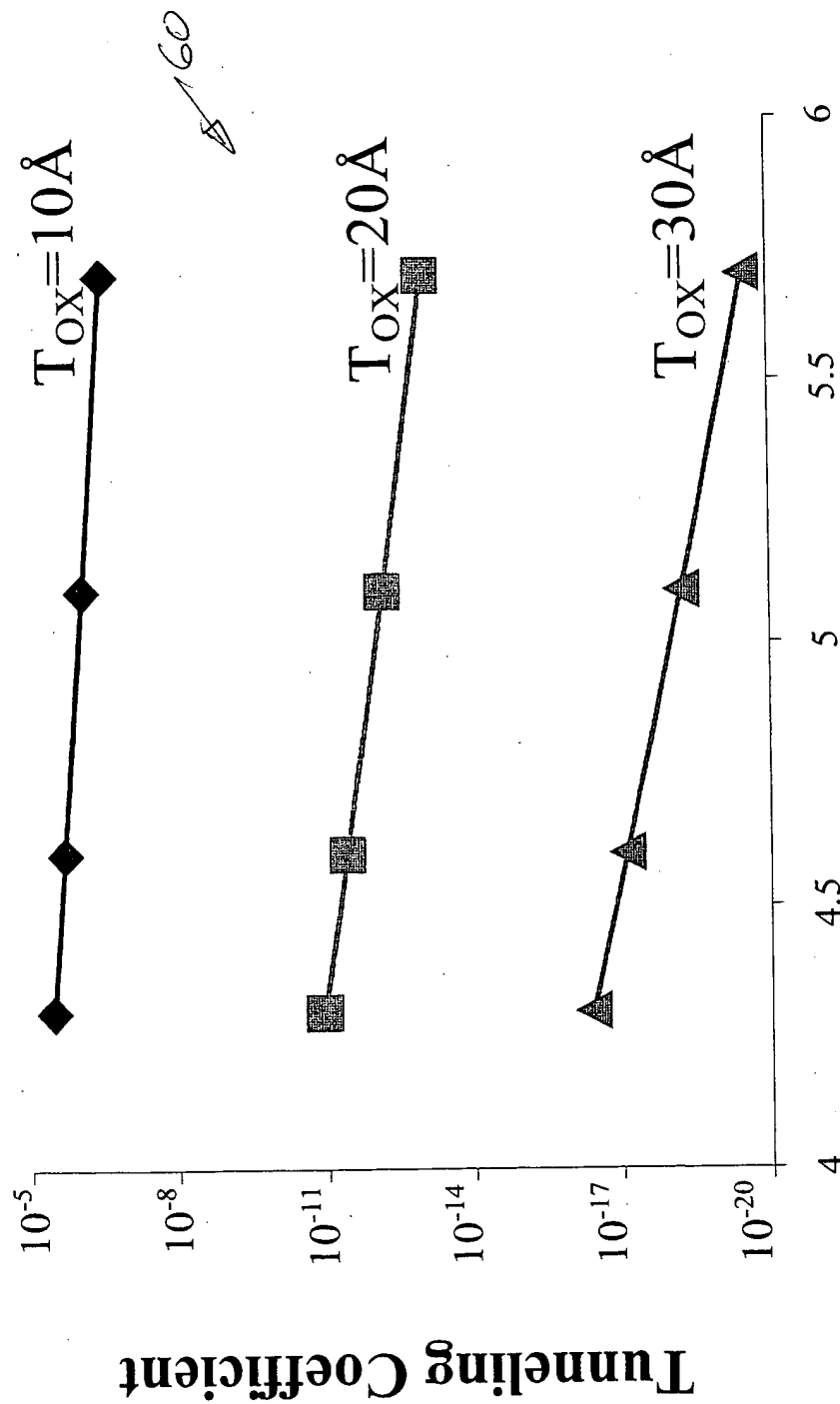


FIG. 3

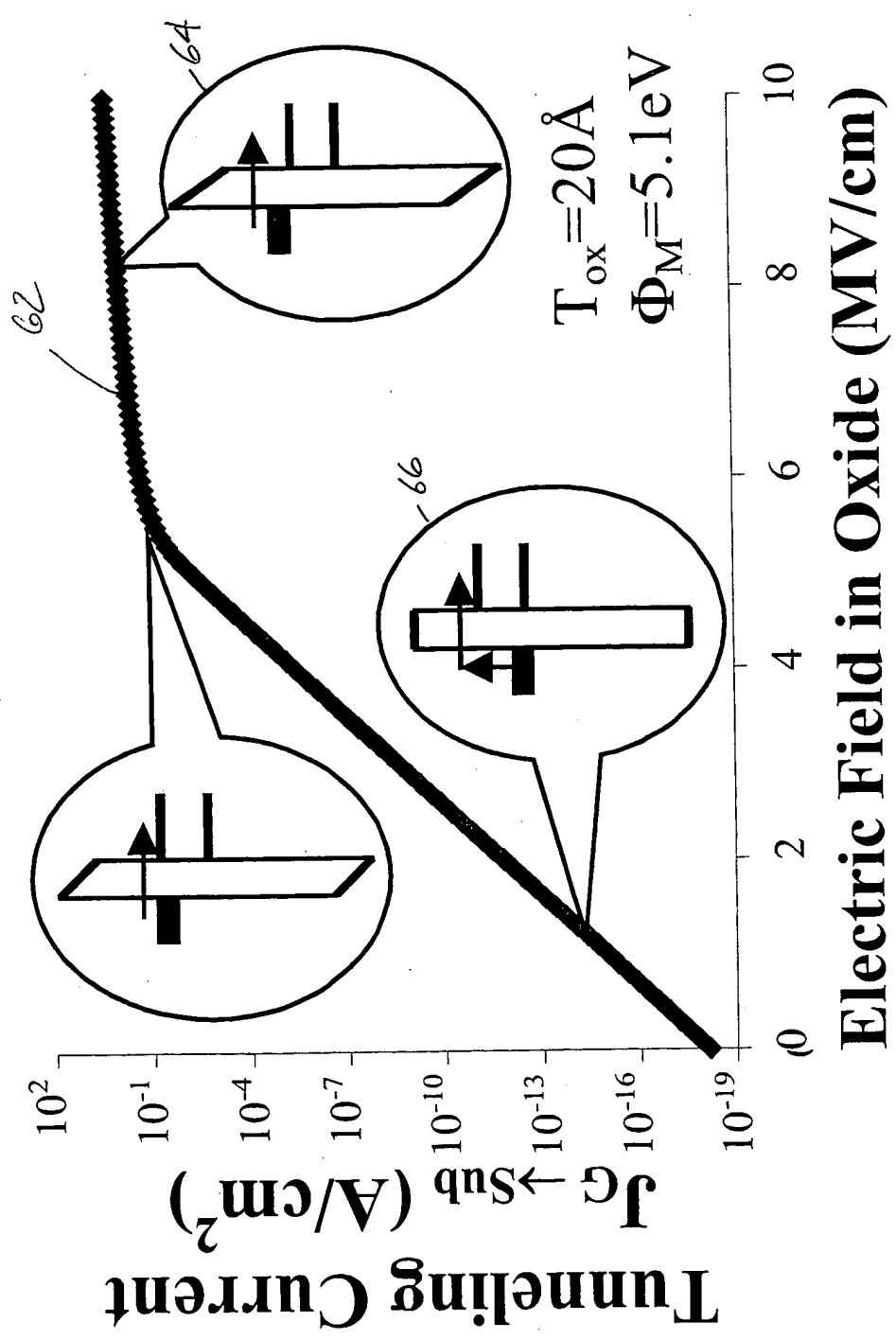


FIG. 4

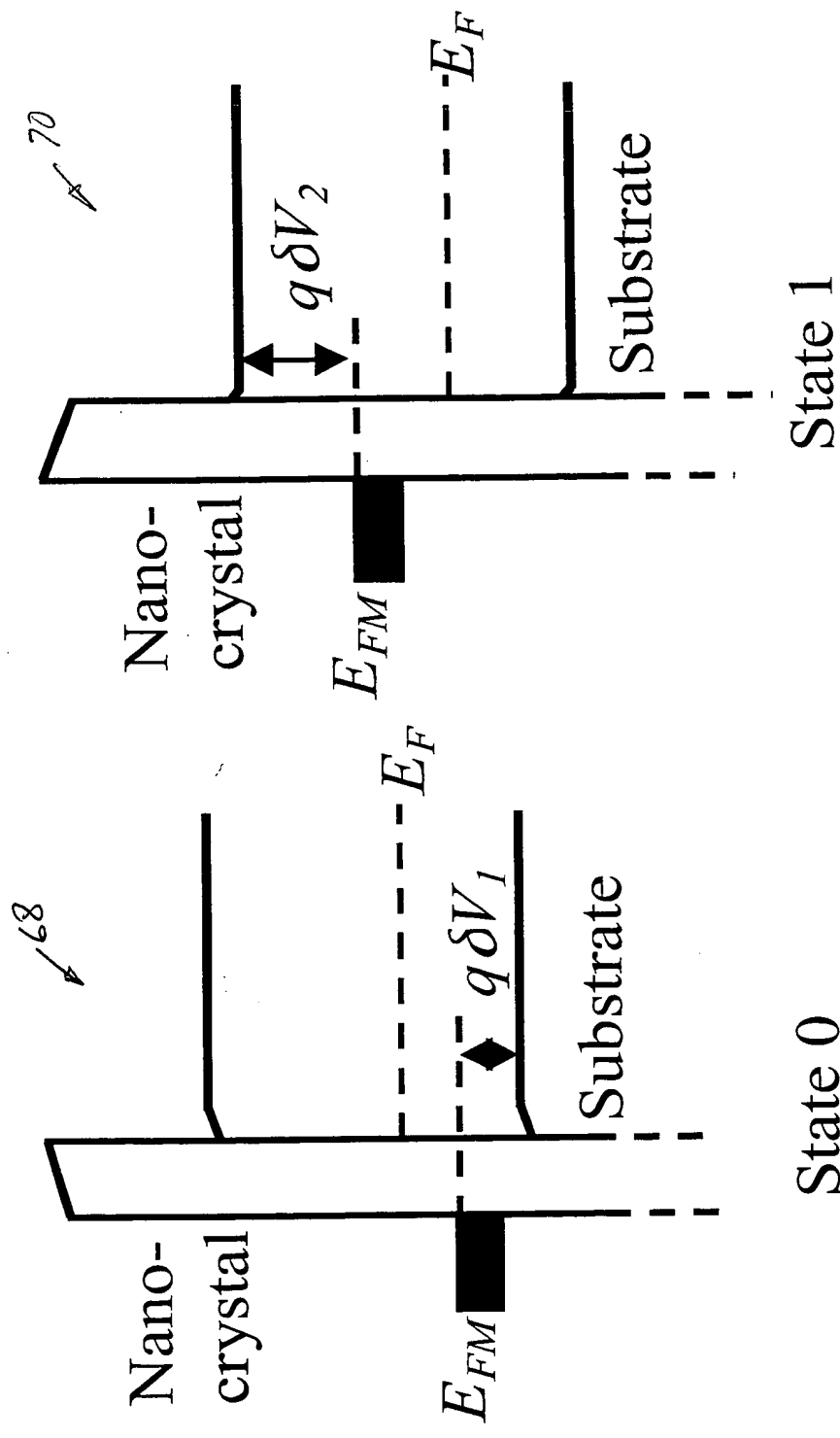


FIG. 5

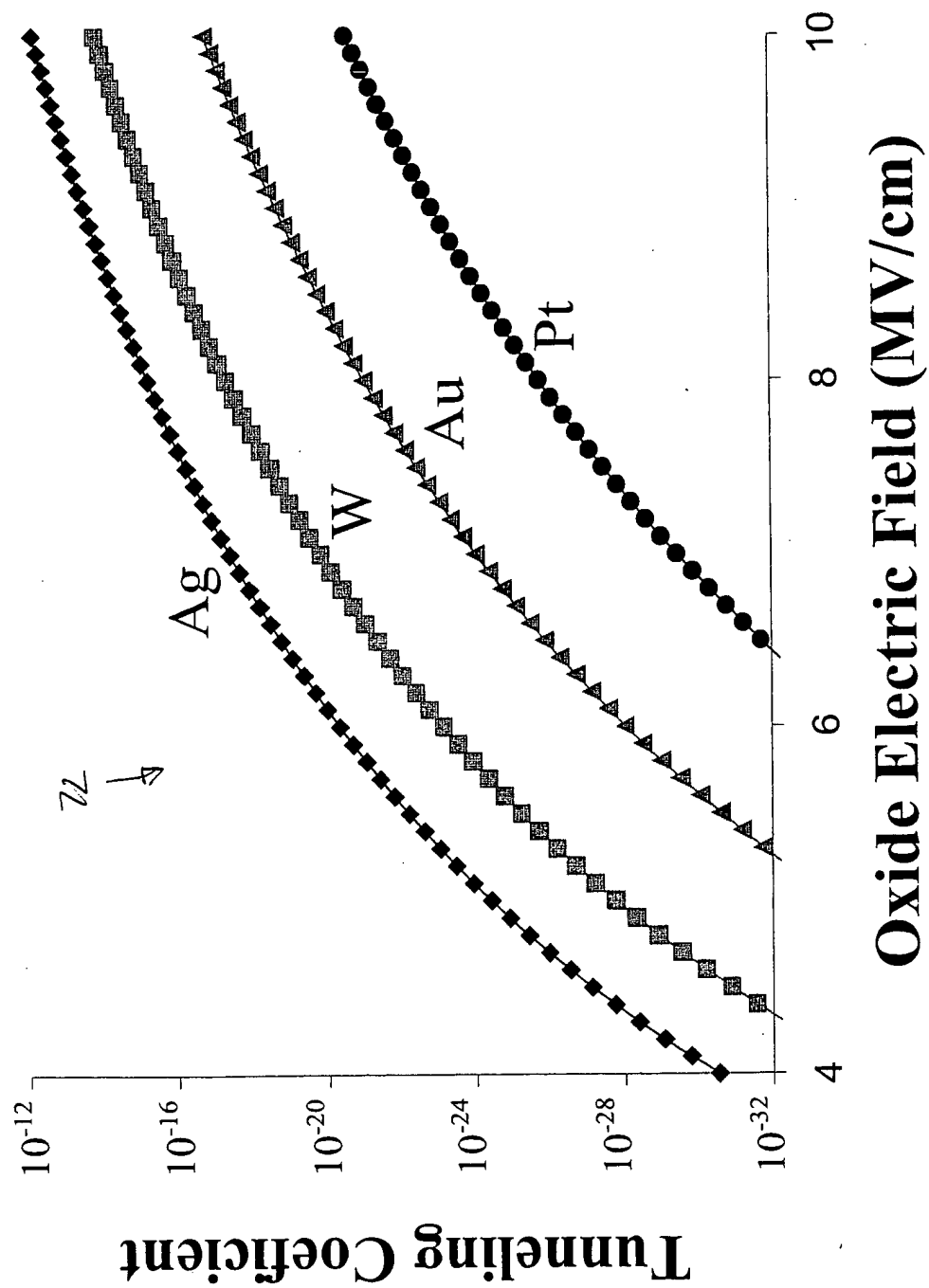


FIG. 6

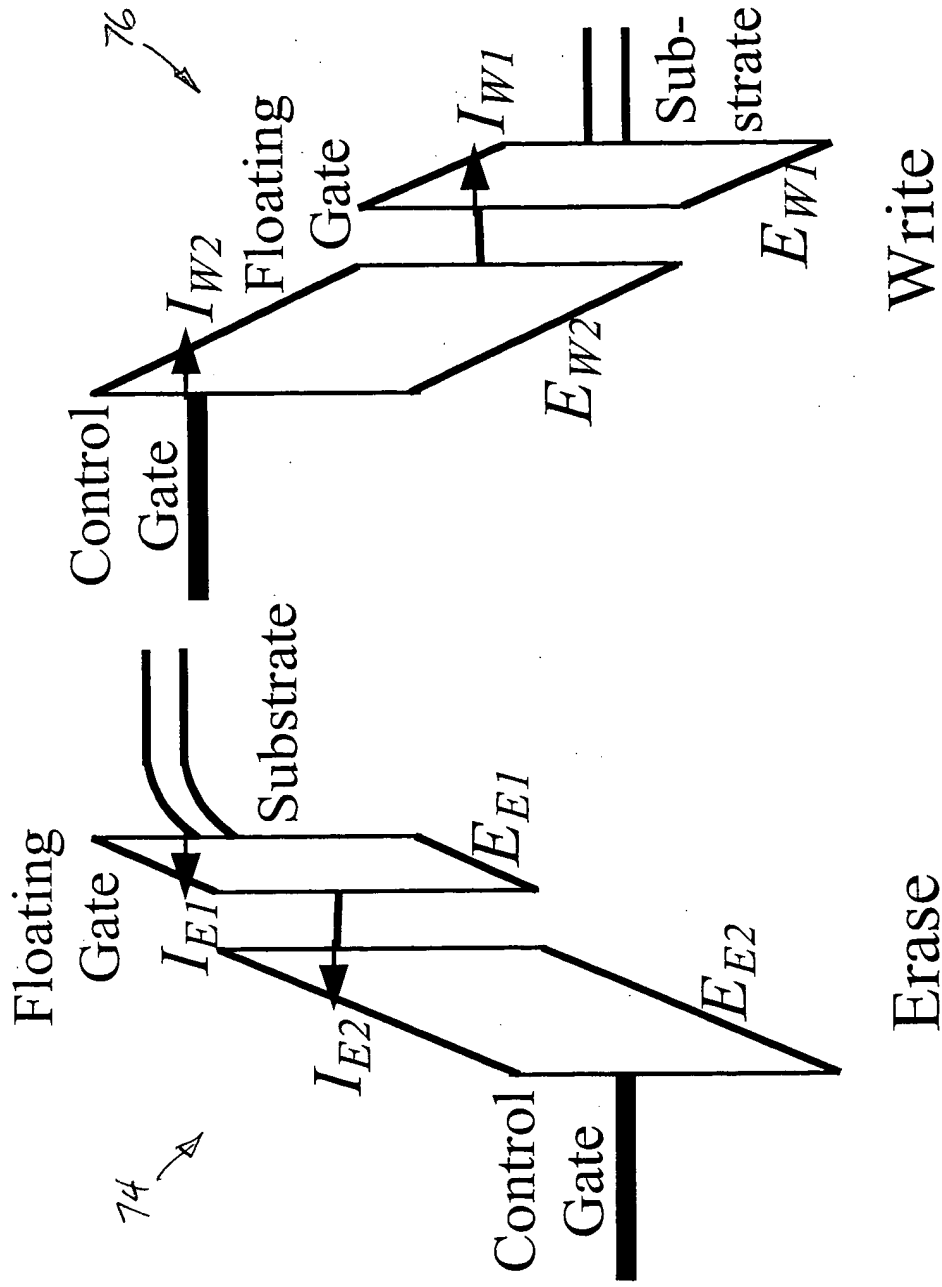


FIG. 7



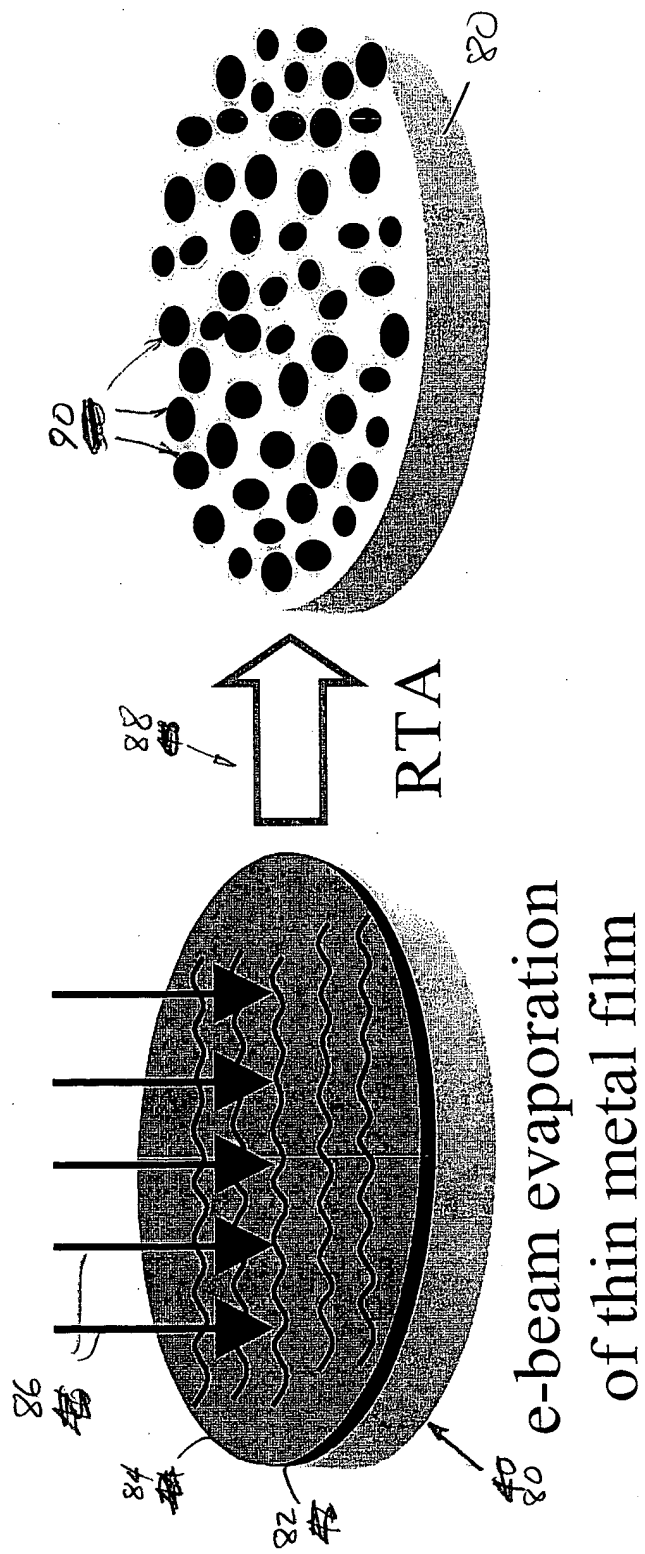


FIG. 8

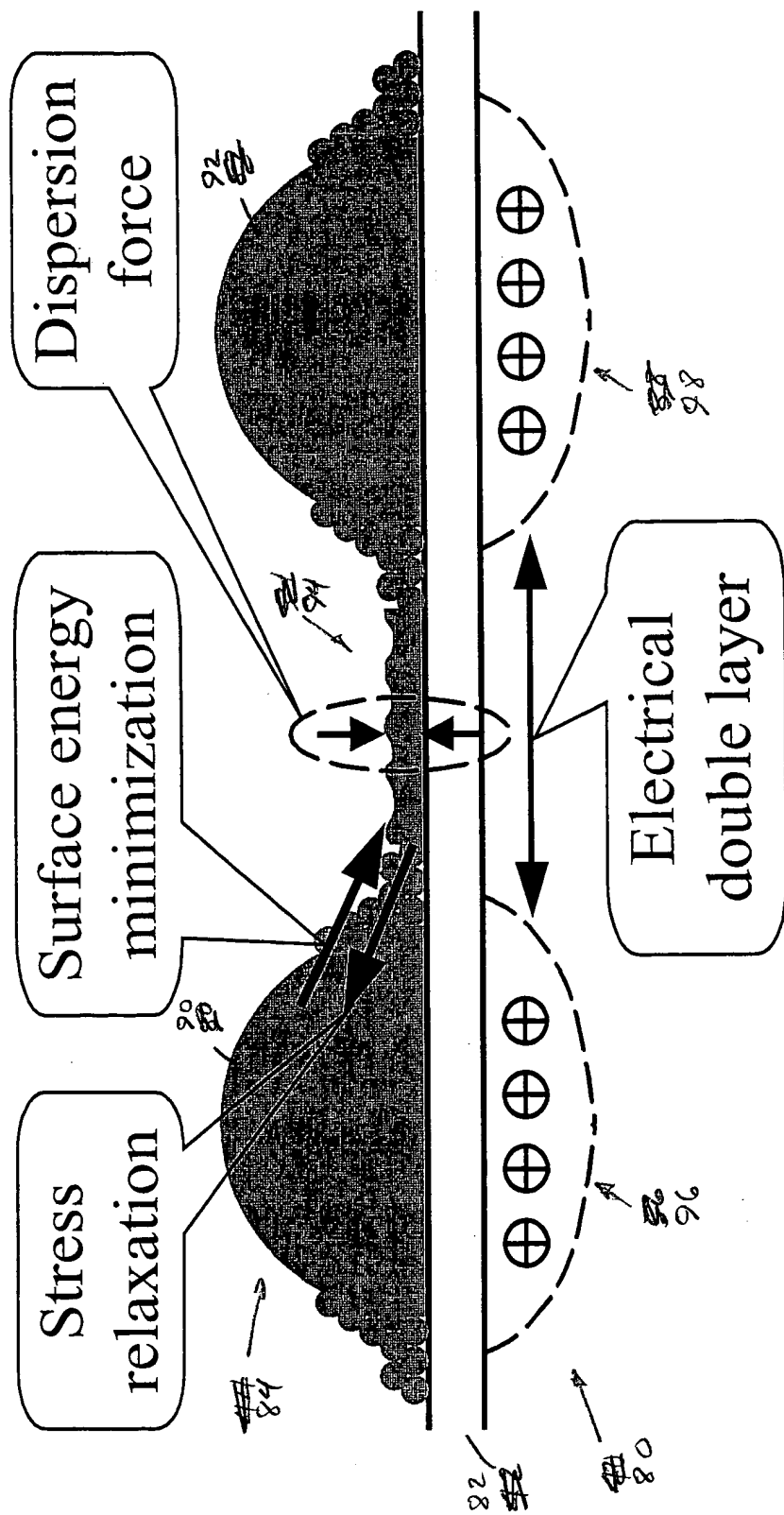


FIG. 9

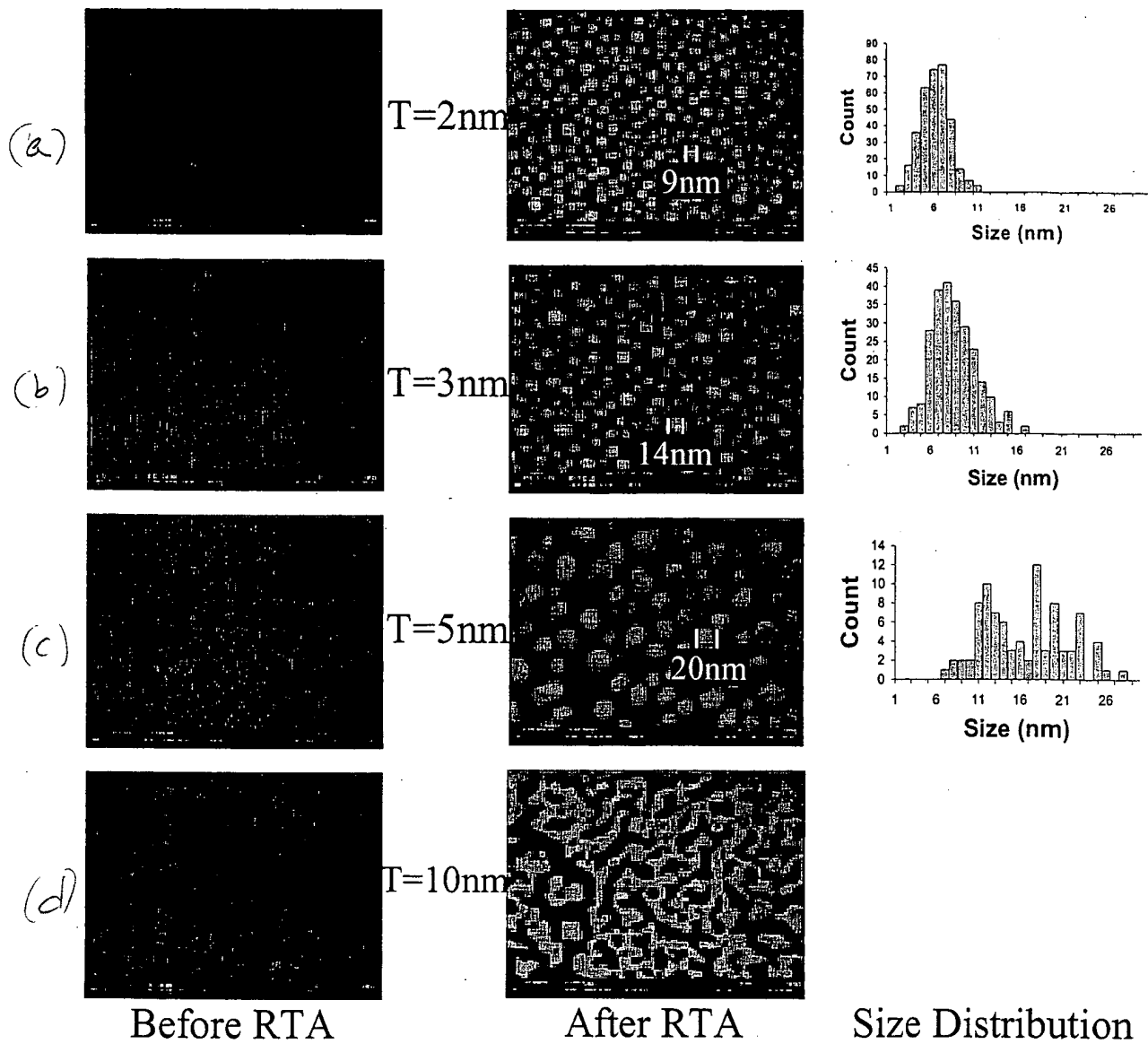
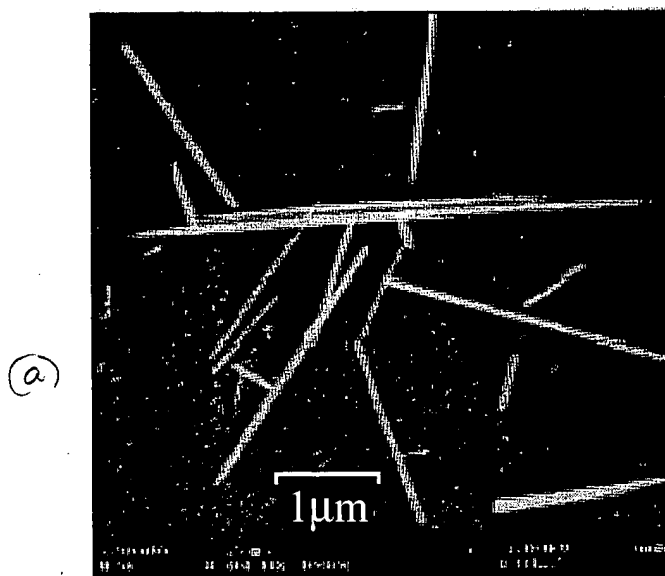
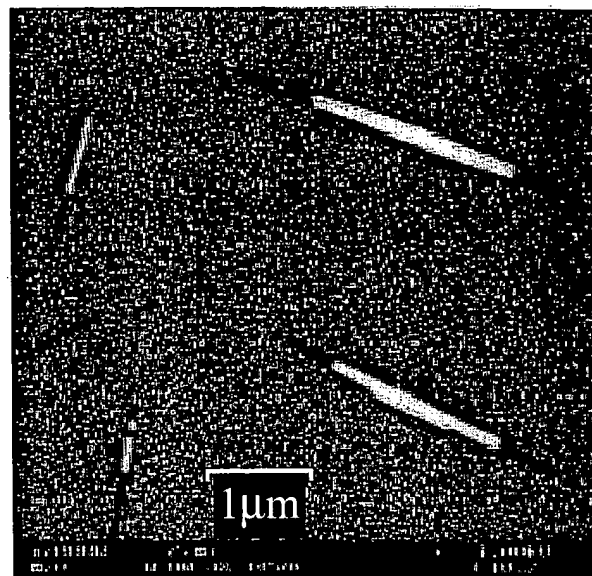


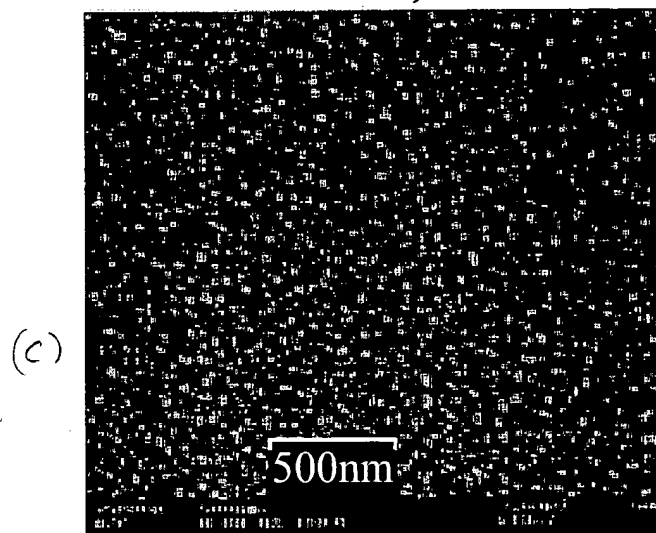
FIG. 10



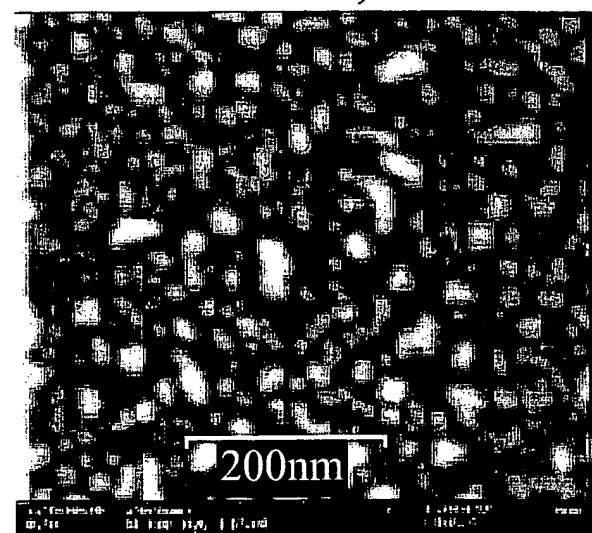
RTA at 950°C, 2 minutes



RTA at 1000°C, 2 minutes

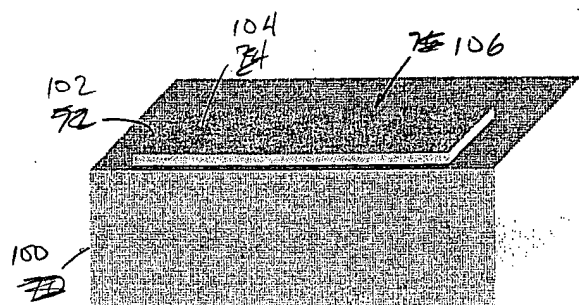


RTA at 1050°C, 2 minutes

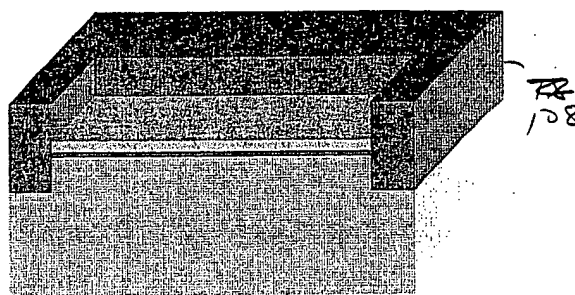


RTA at 1100°C, 2 minutes

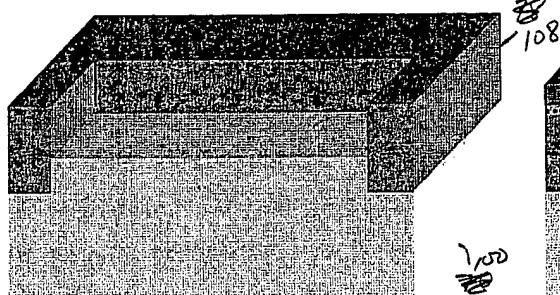
FIG. 11



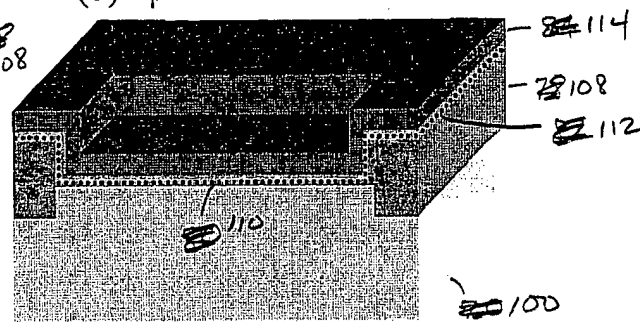
(a) Definition of active region



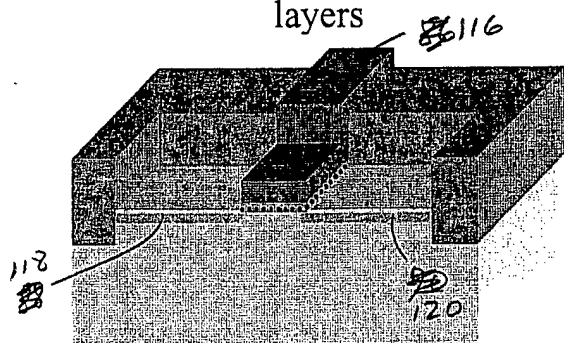
(b) 1 $\mu$ m field oxidation



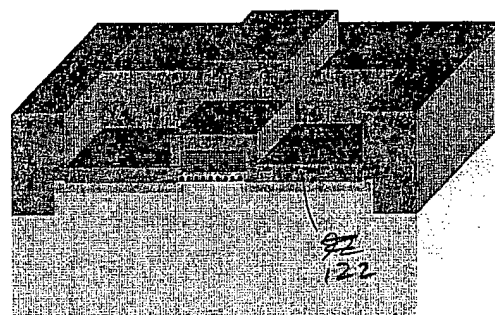
(c) Stripping nitride and pad oxide layers



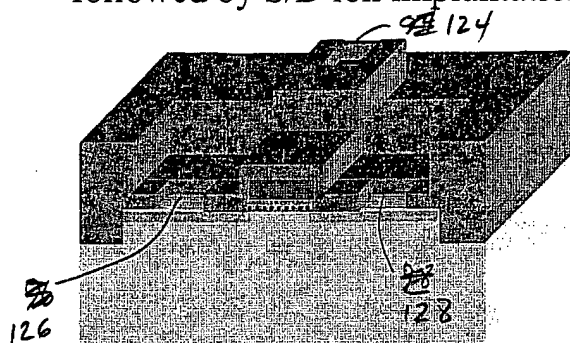
(d) Gate stack formation



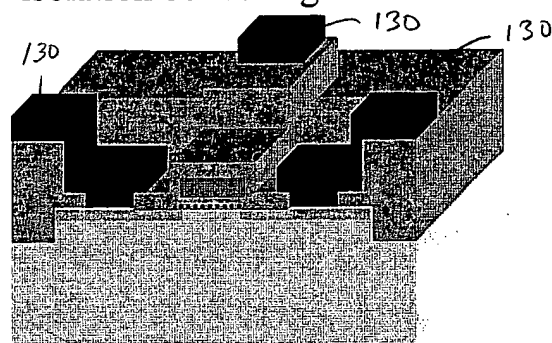
(e) Definition of gate pattern followed by S/D ion implantation



(f) PECVD oxide deposition for isolation between gate and S/D



(g) Etching contact window



(h) W sputtering and etching for final metalization

FIG. 12

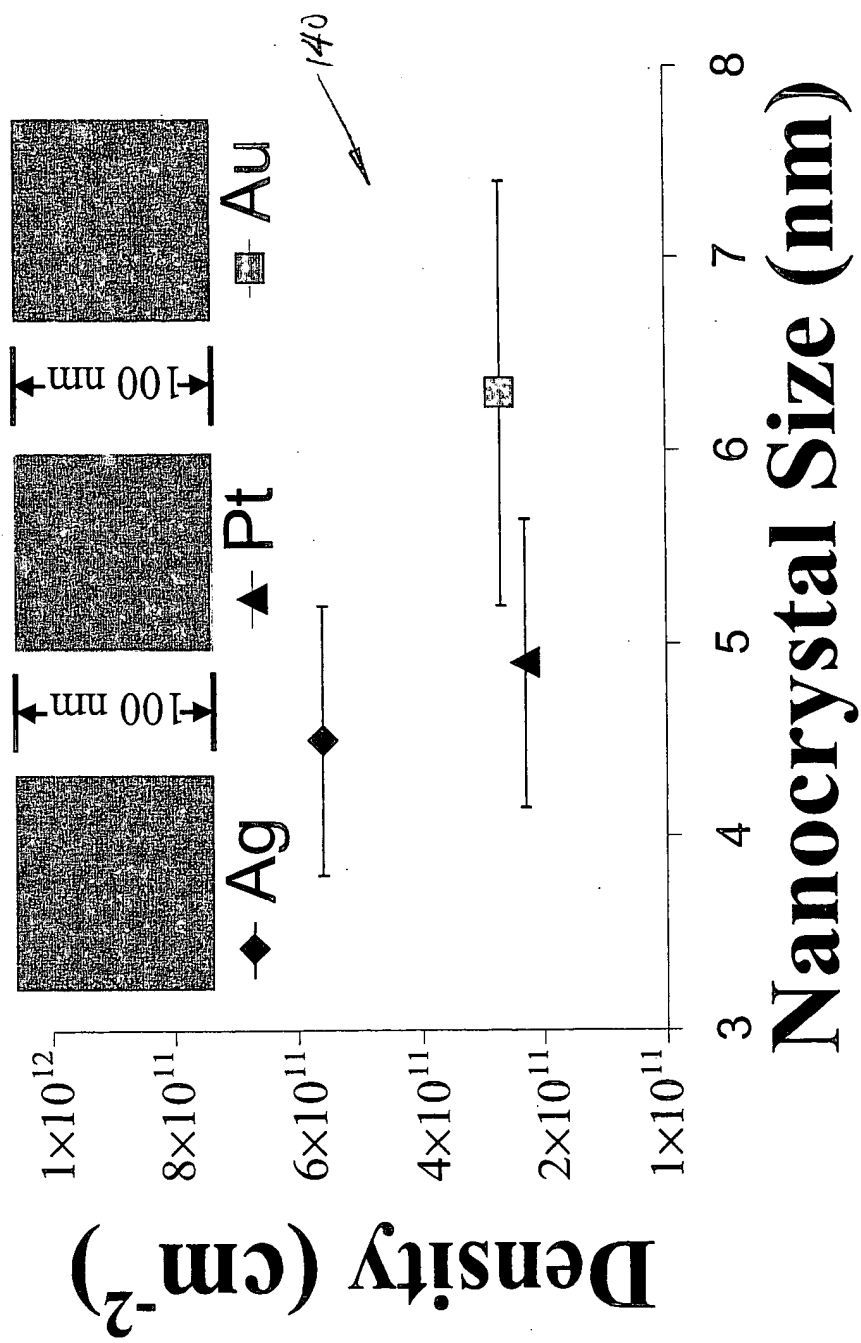
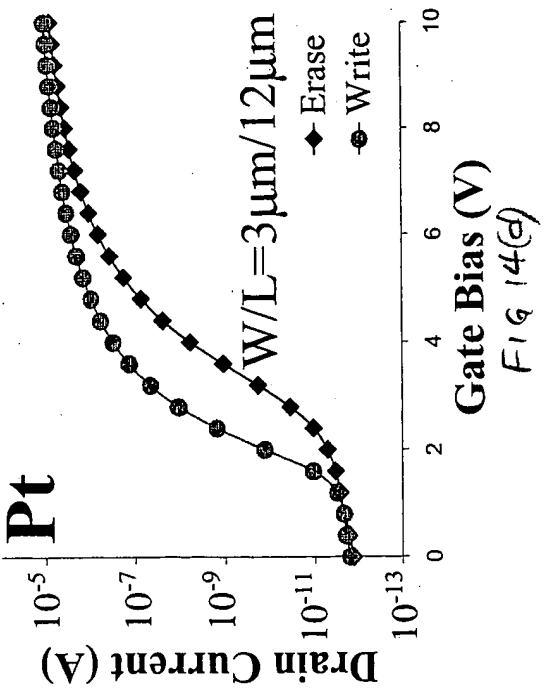
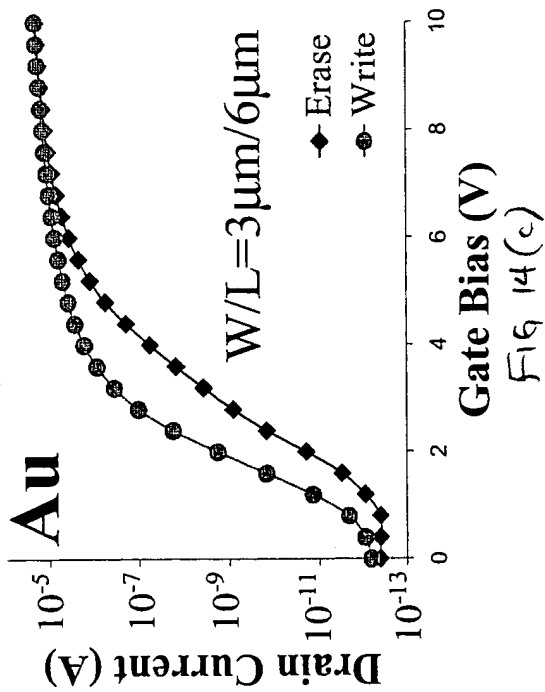
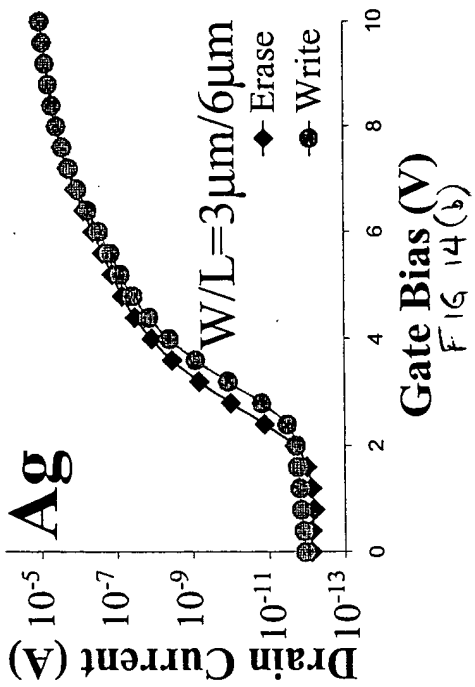
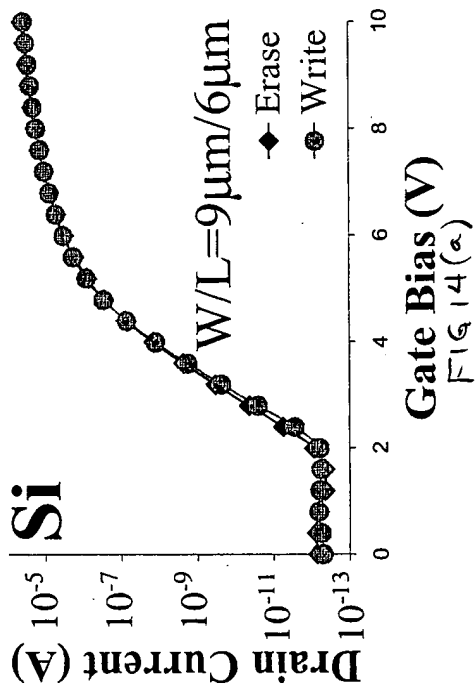


FIG 13



**FIG 14**

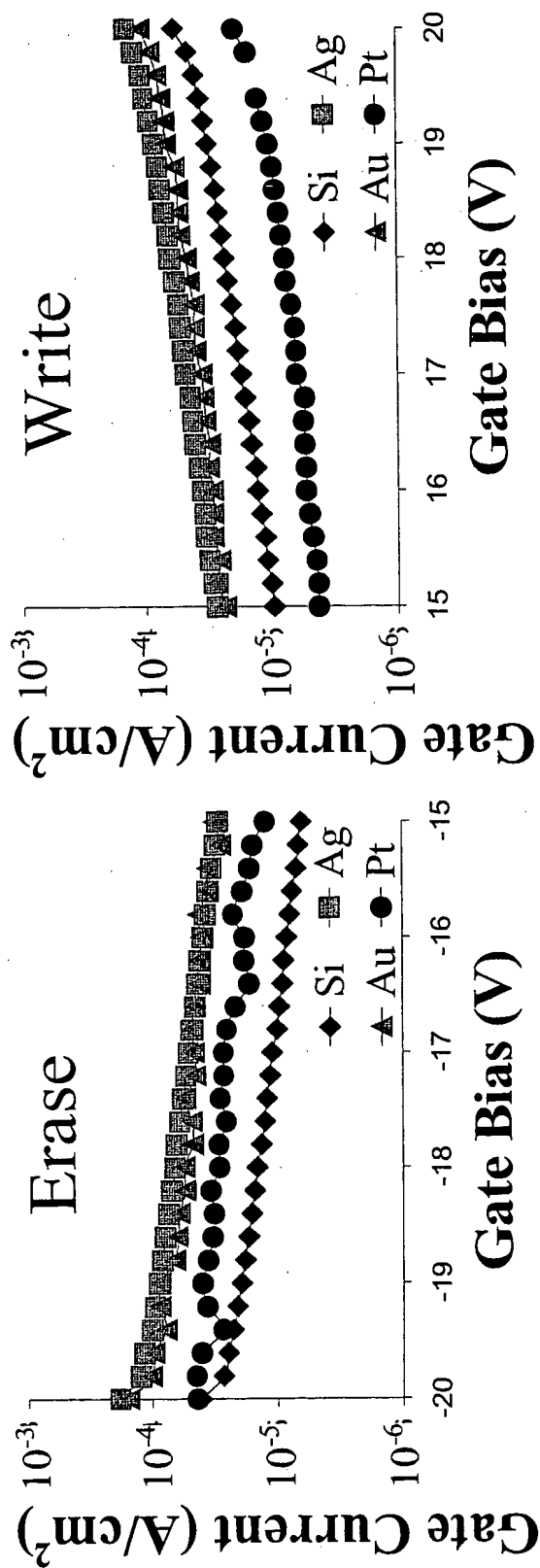


FIG. 15



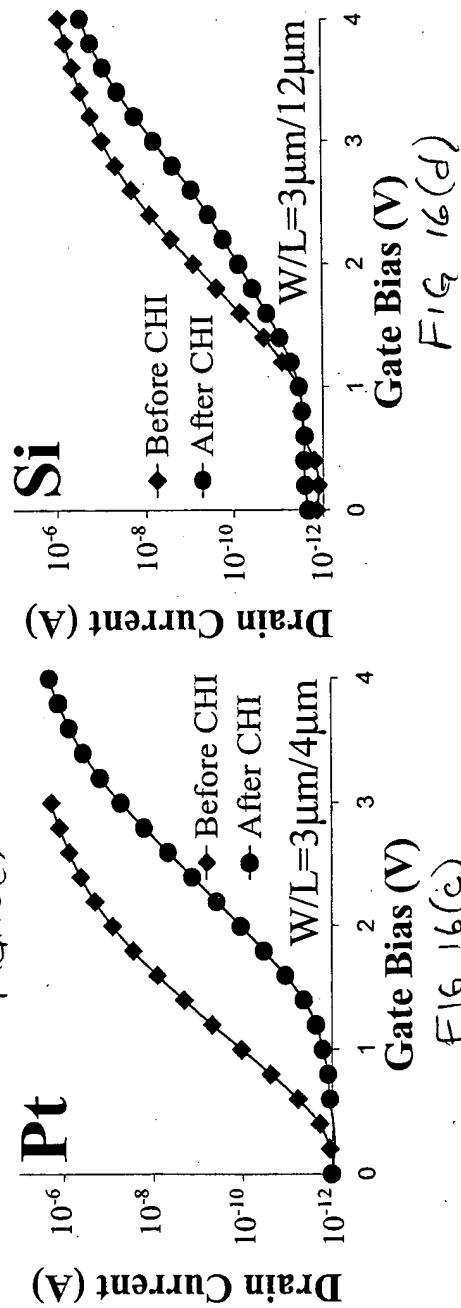
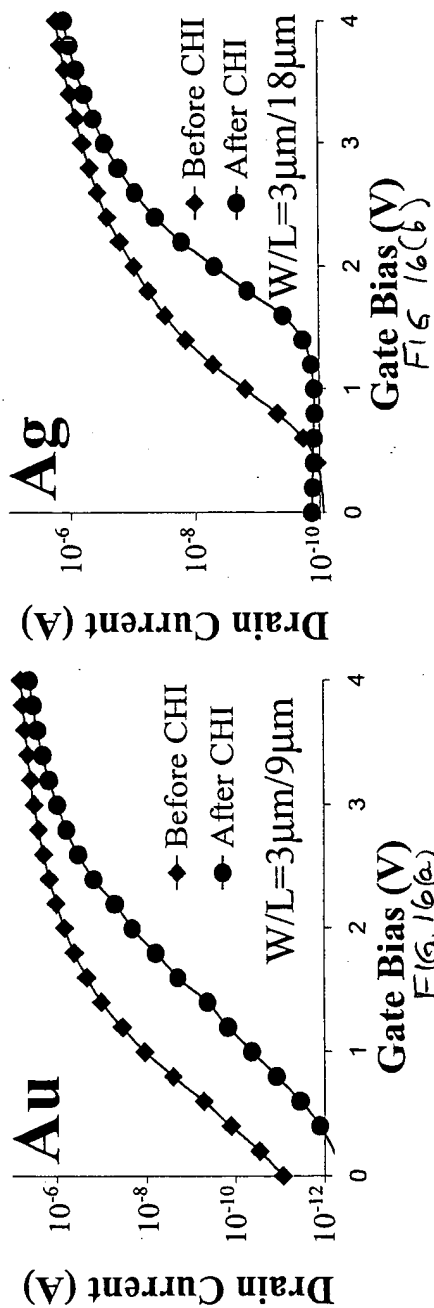


FIG 16(c)

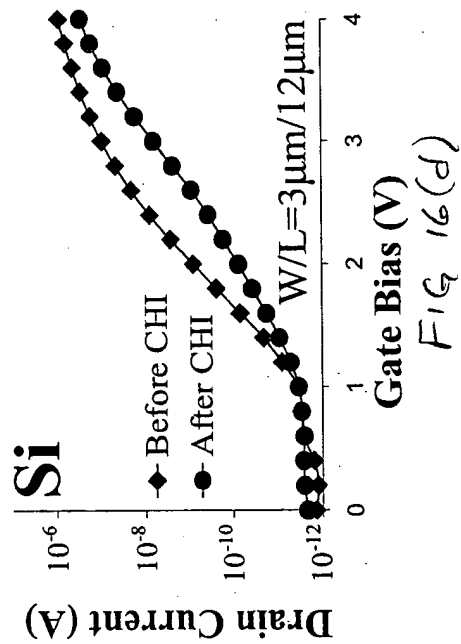
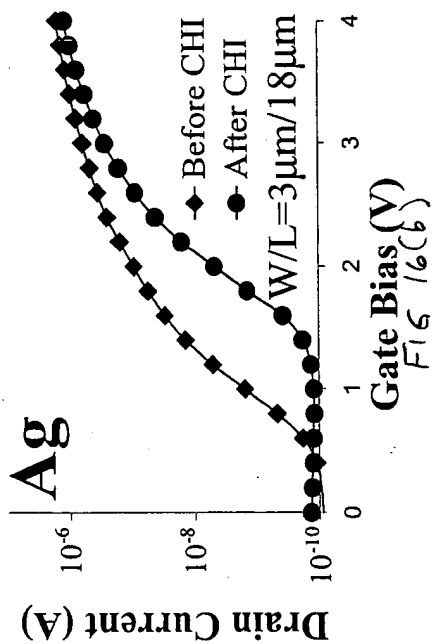


FIG 16(d)

~~FIG 16~~

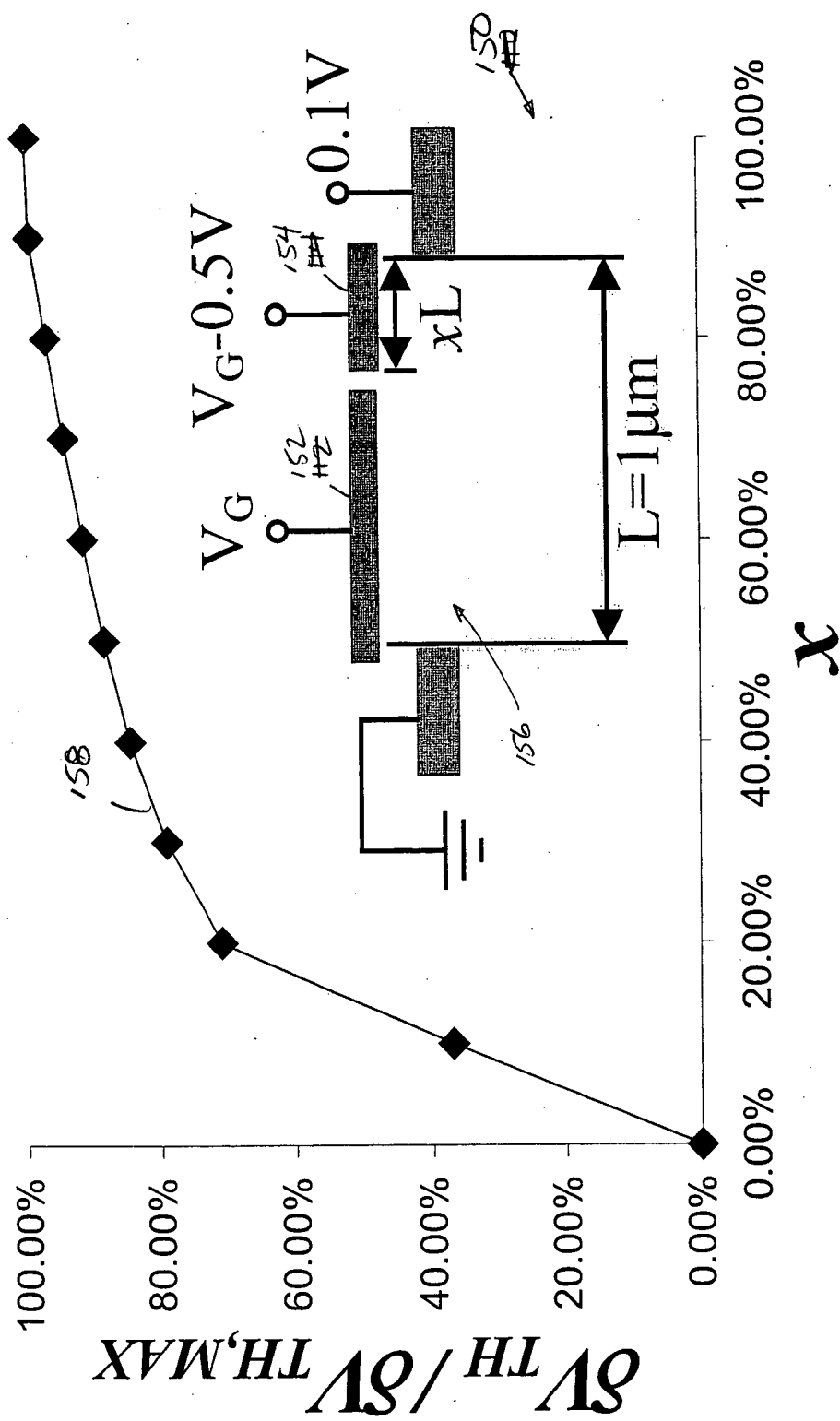


FIG 17

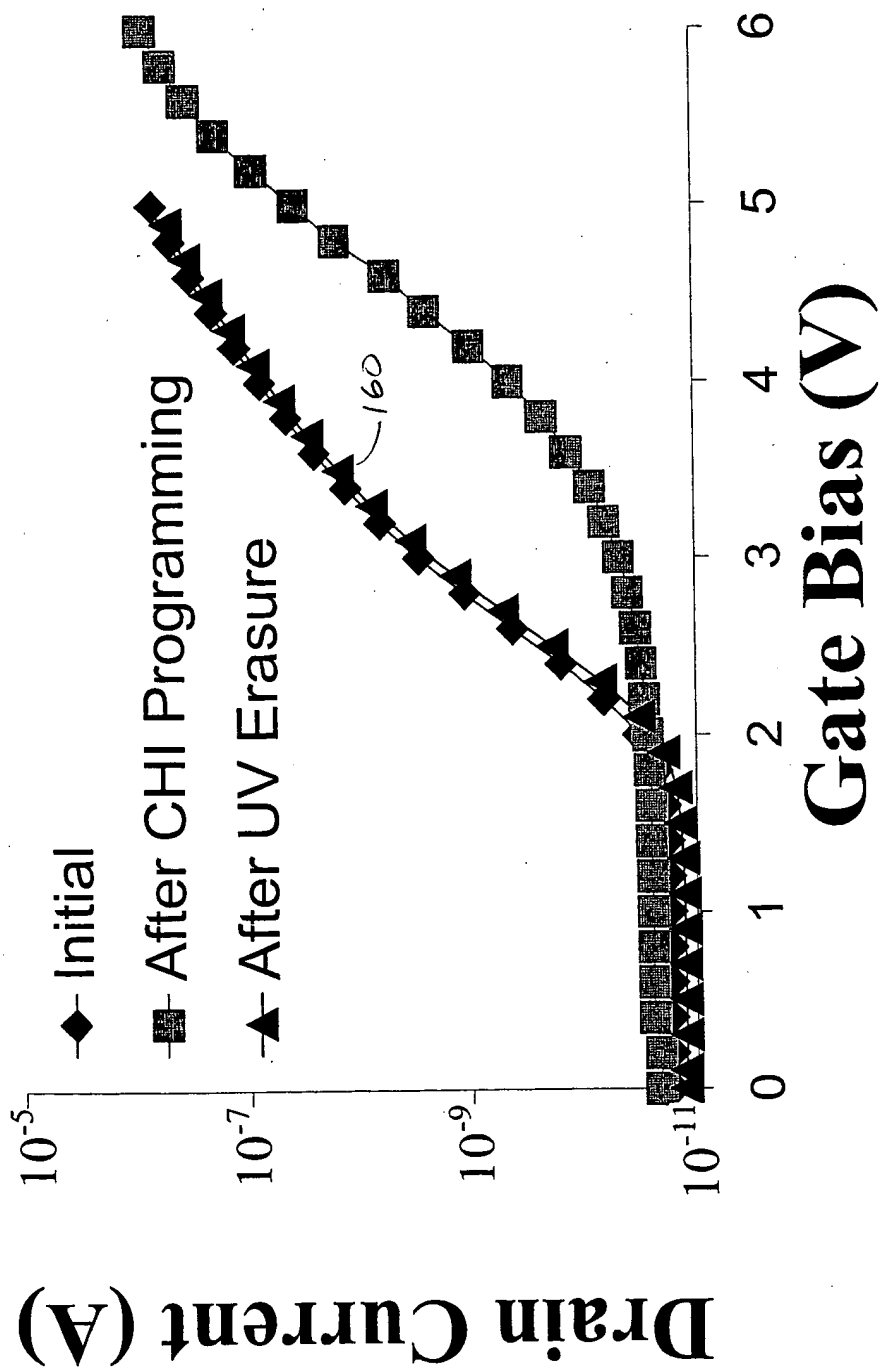


FIG 18

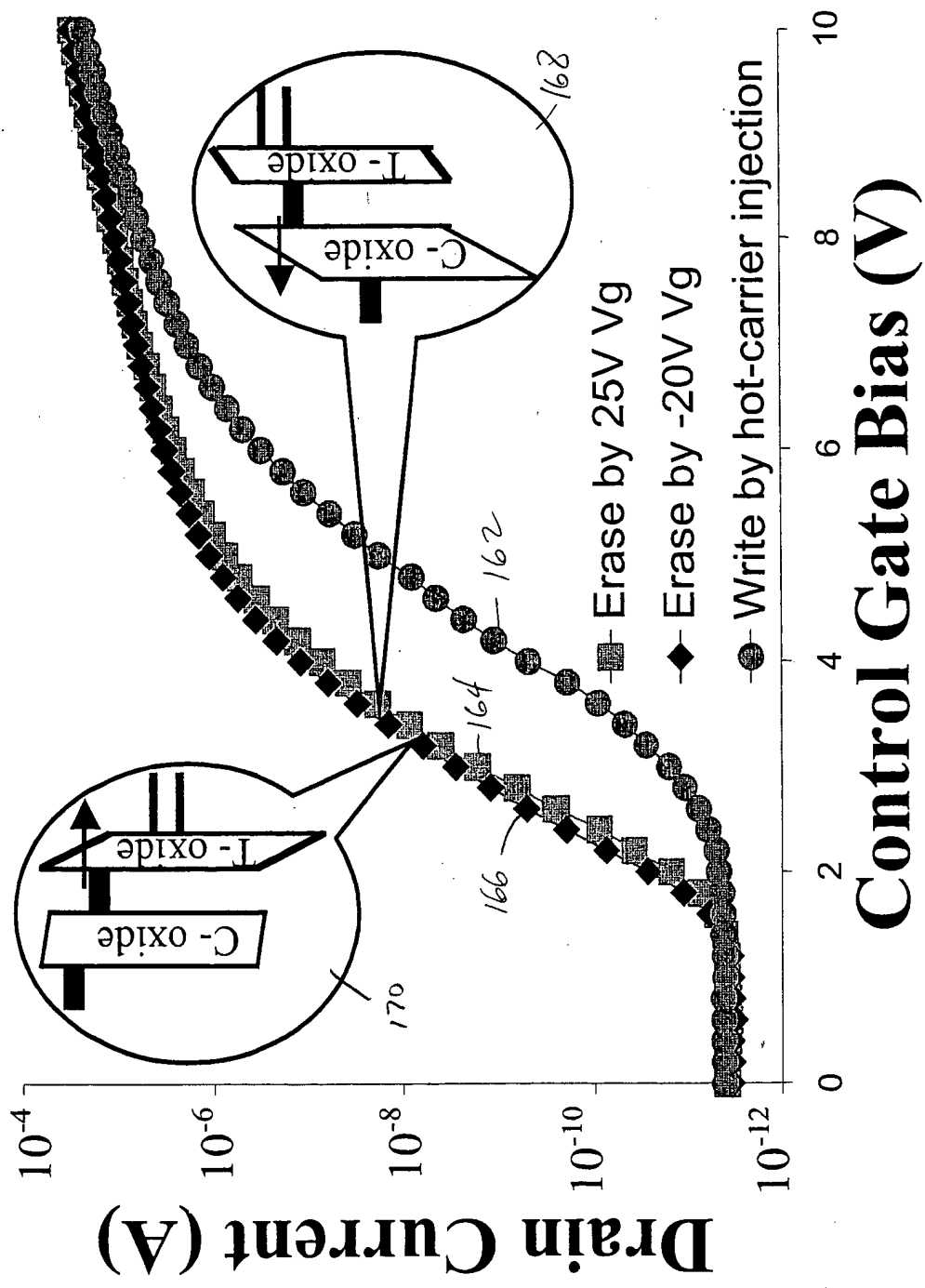


FIG 19

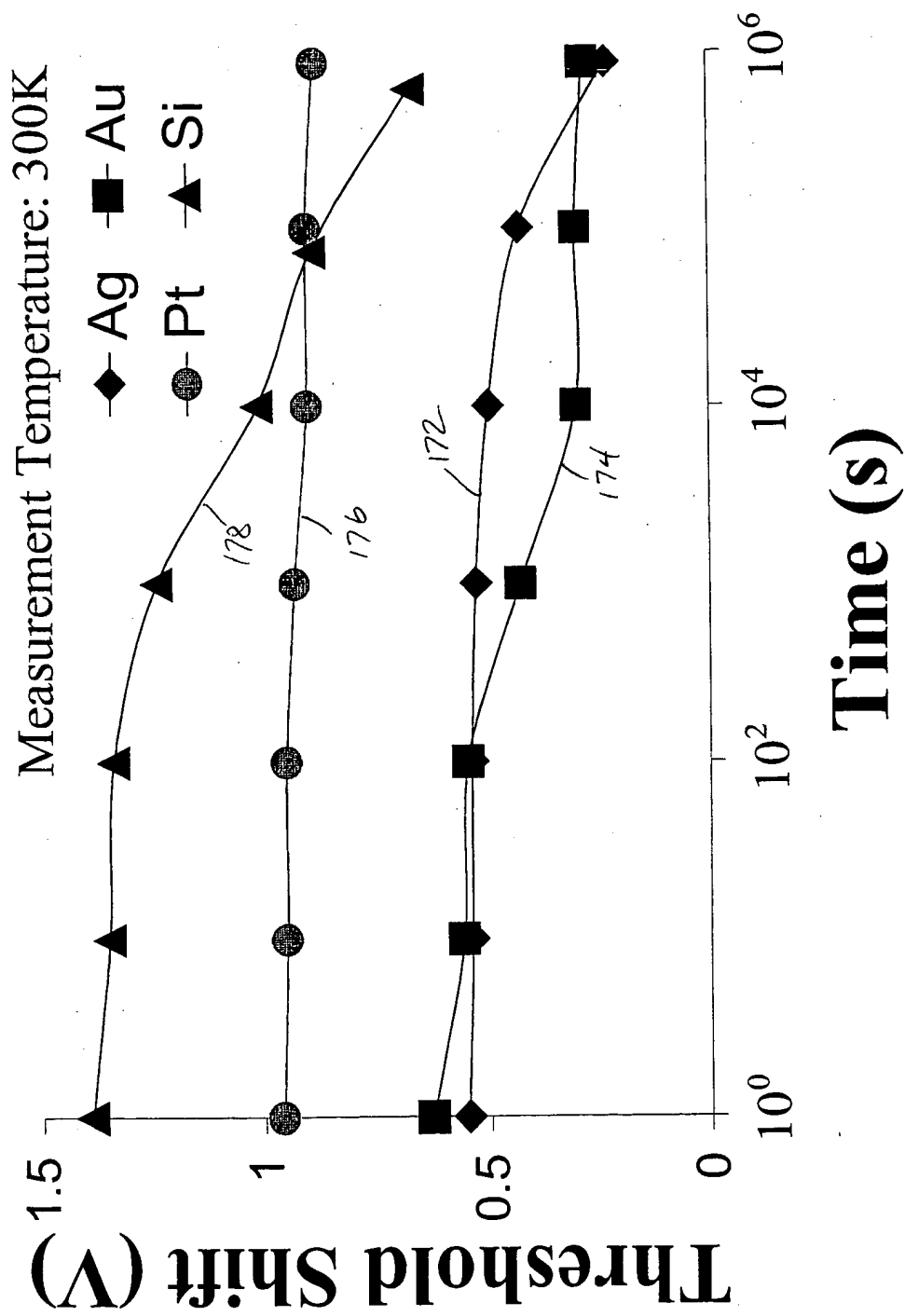
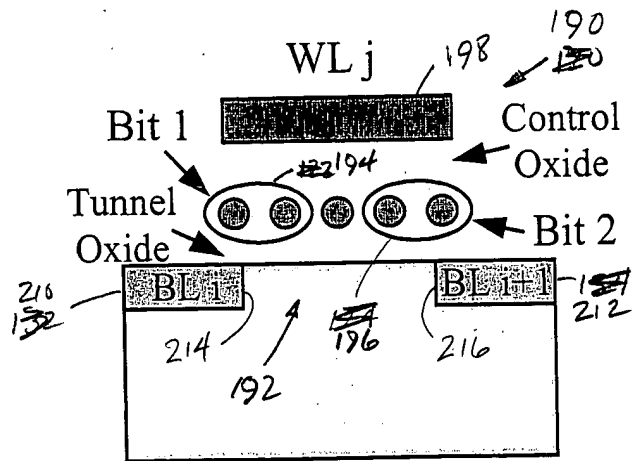
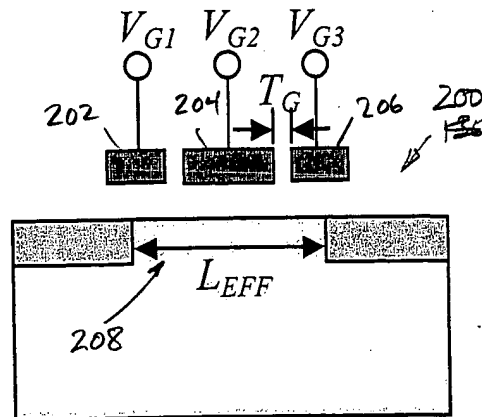


FIG 20



Nanocrystal  
Memory

FIG. 21(a)



Split-gate  
MOSFET

Fig 21(b)

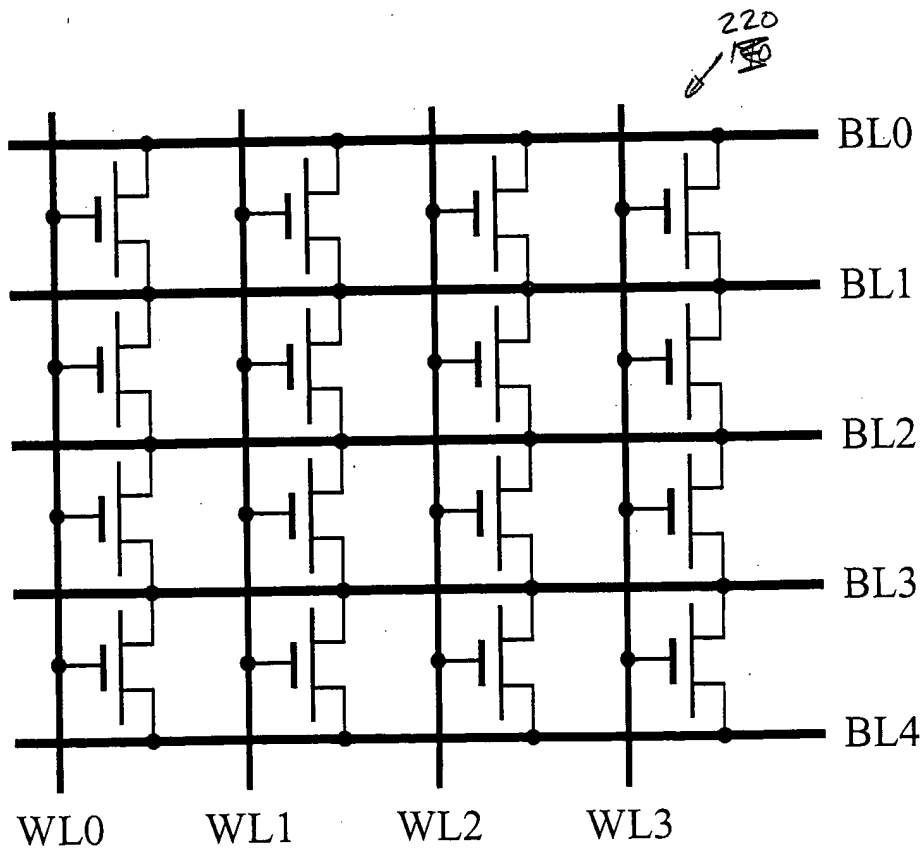


FIG. 21(b)(c)

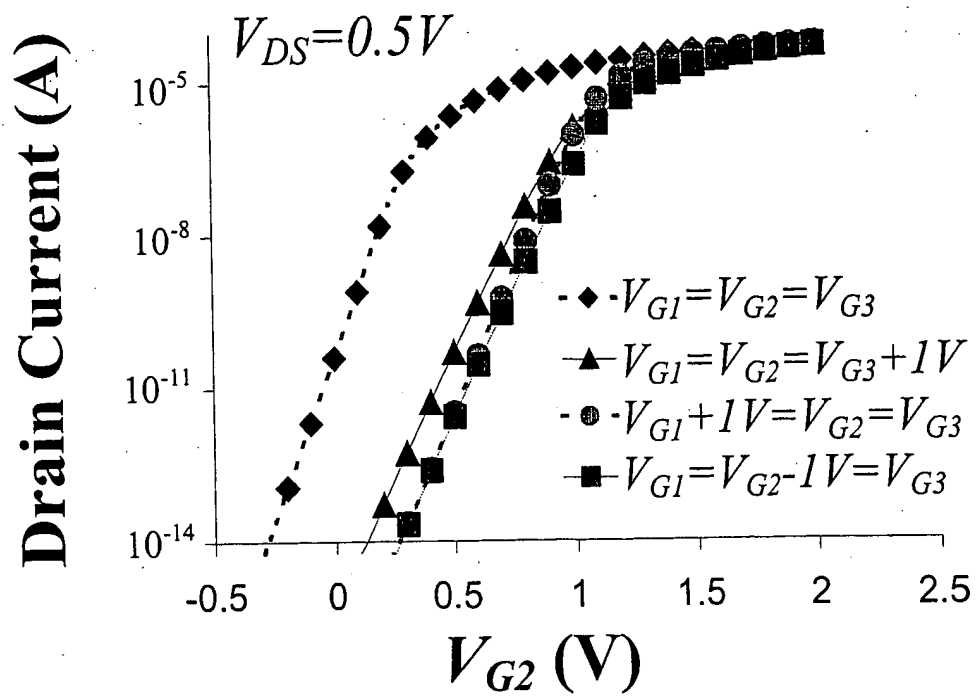


FIG. 22(a)

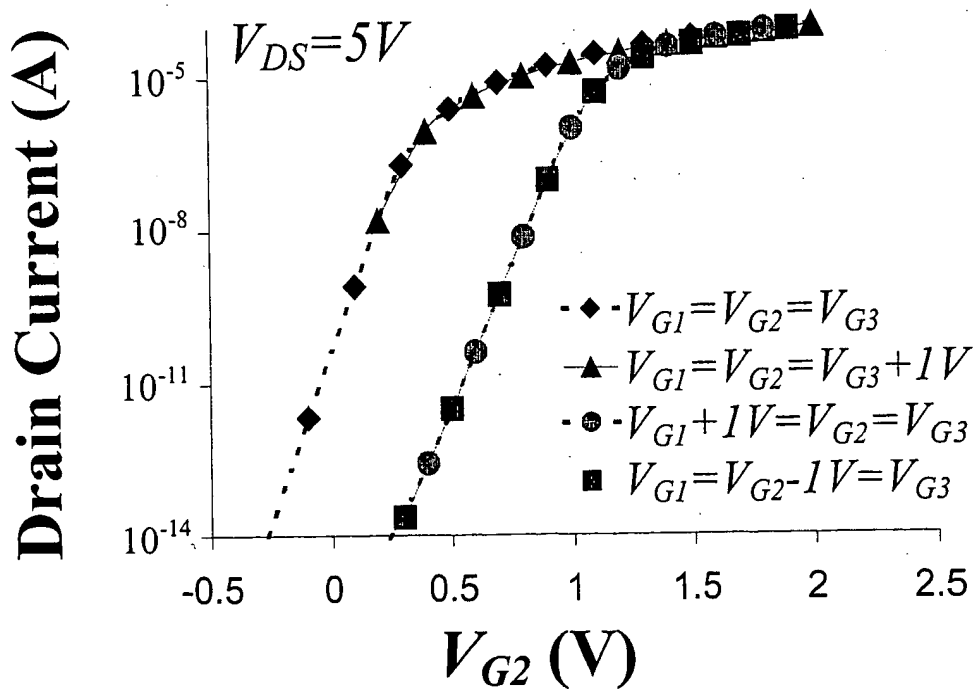


FIG. 22(b)

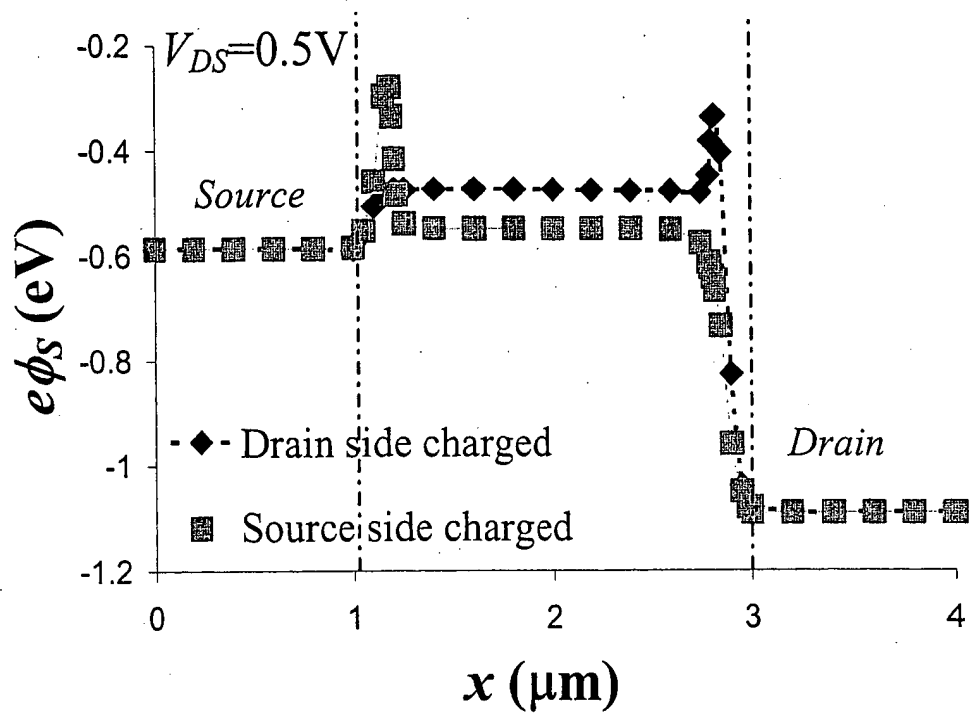


FIG 23(a)

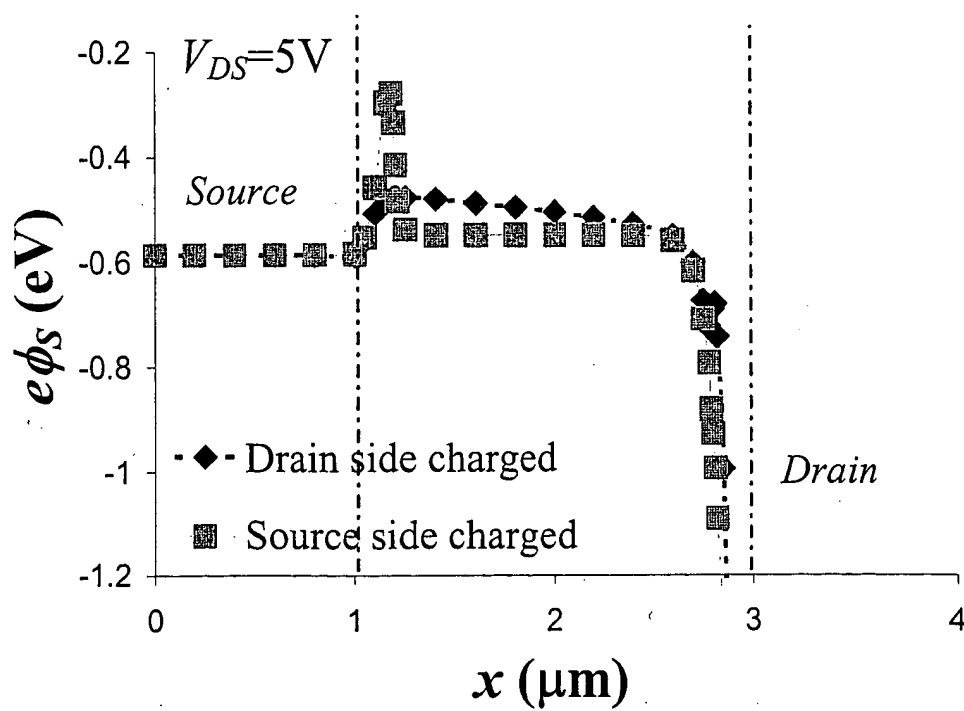


FIG 23(b)



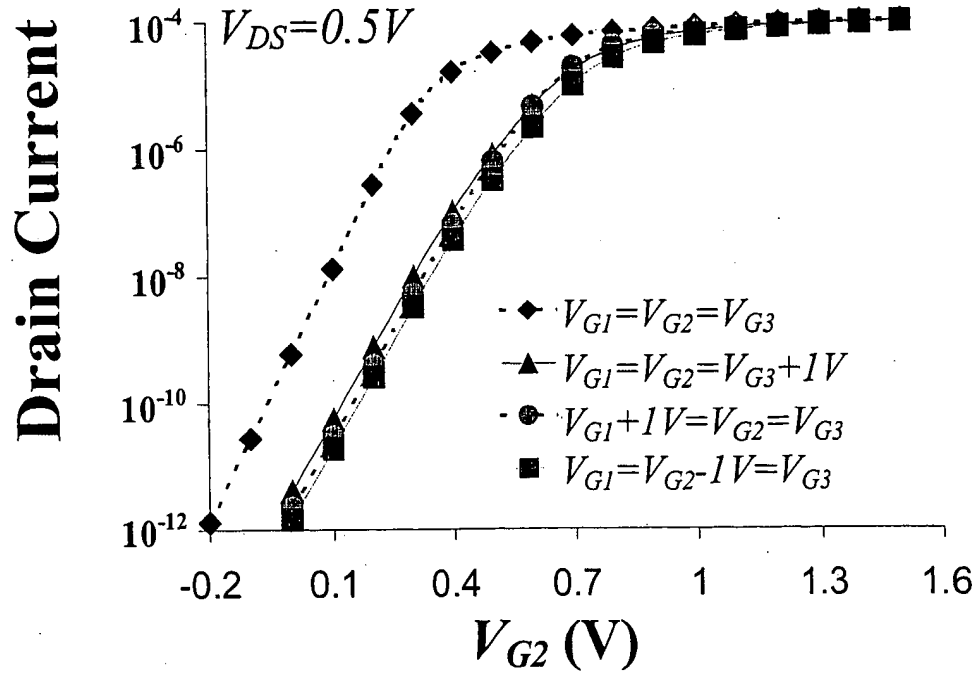


FIG. 24(a)

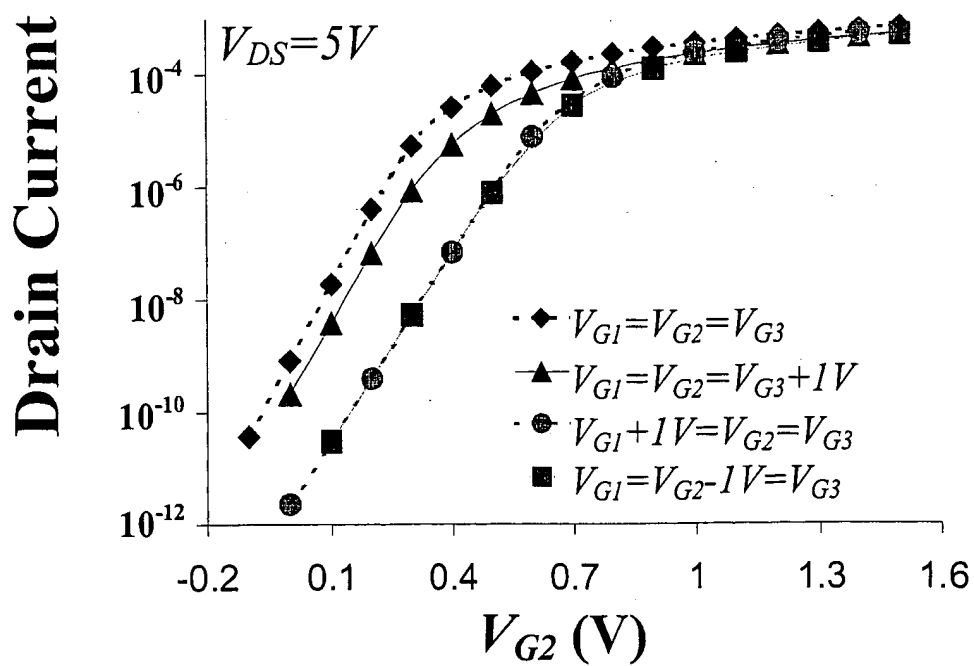


FIG. 24(b)

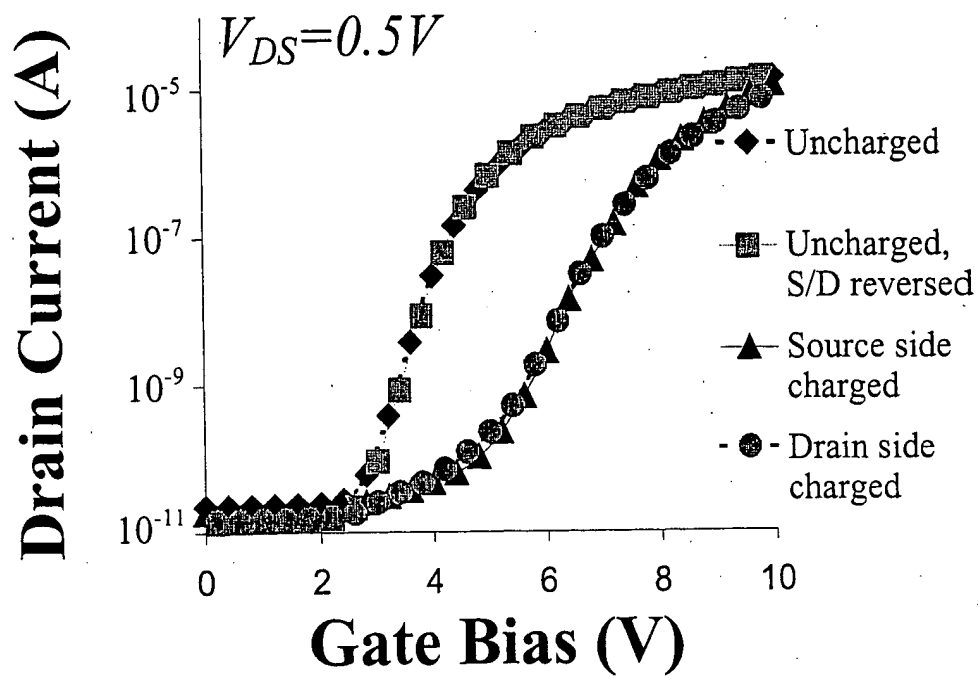


FIG. 25(a)

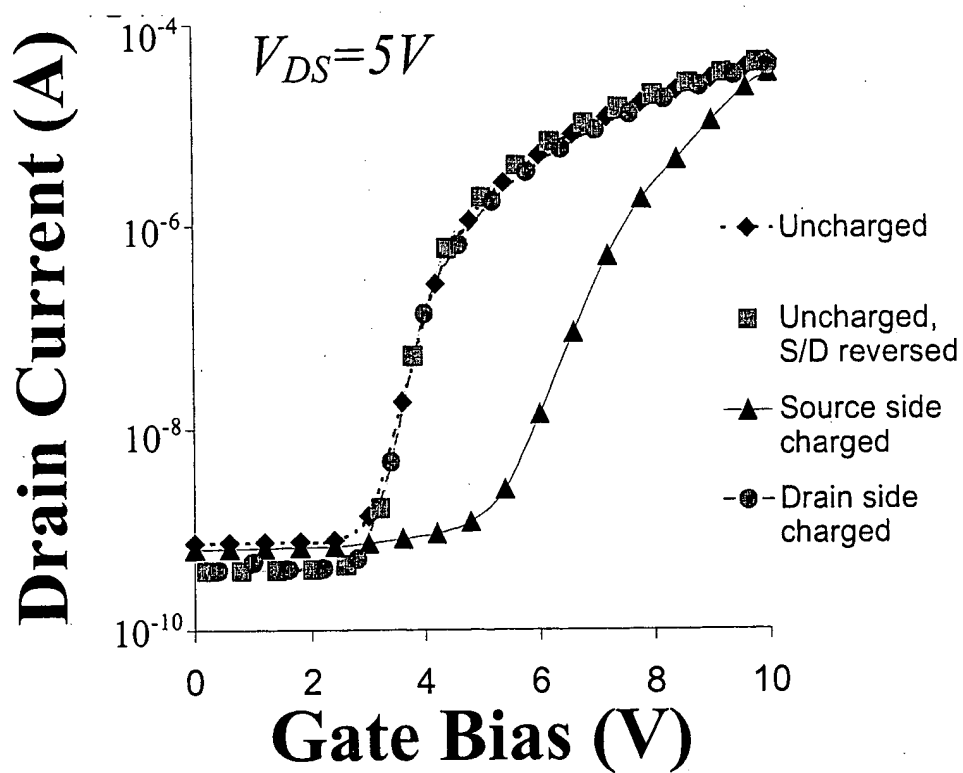
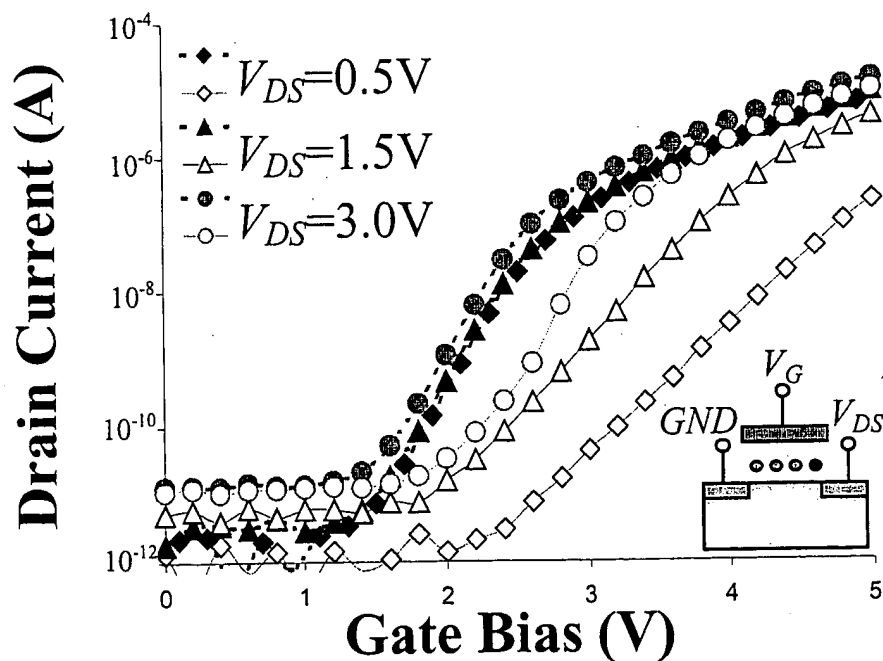
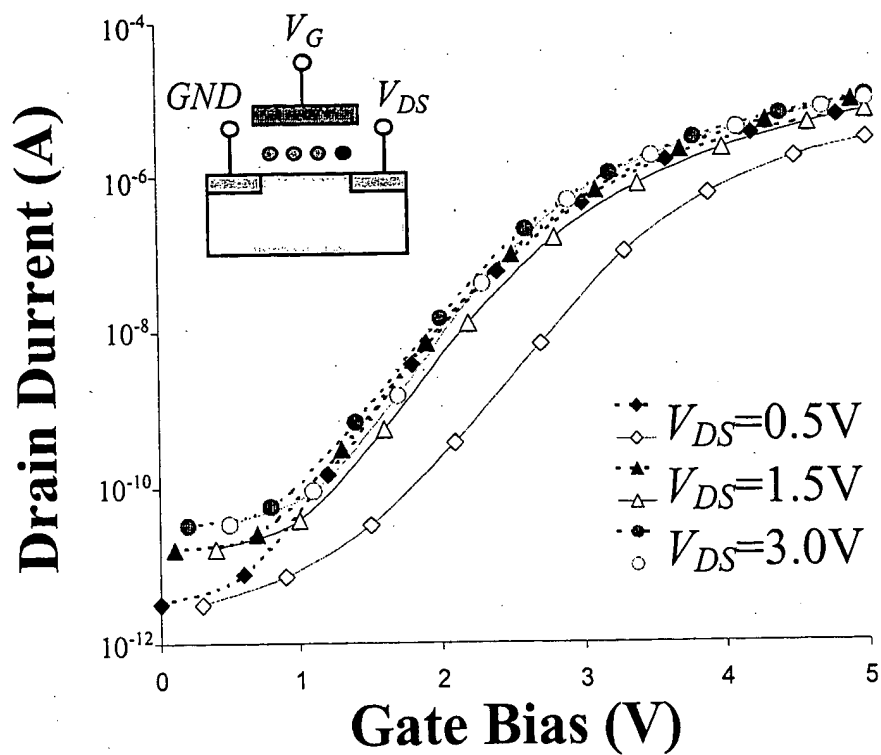


FIG. 25(b)



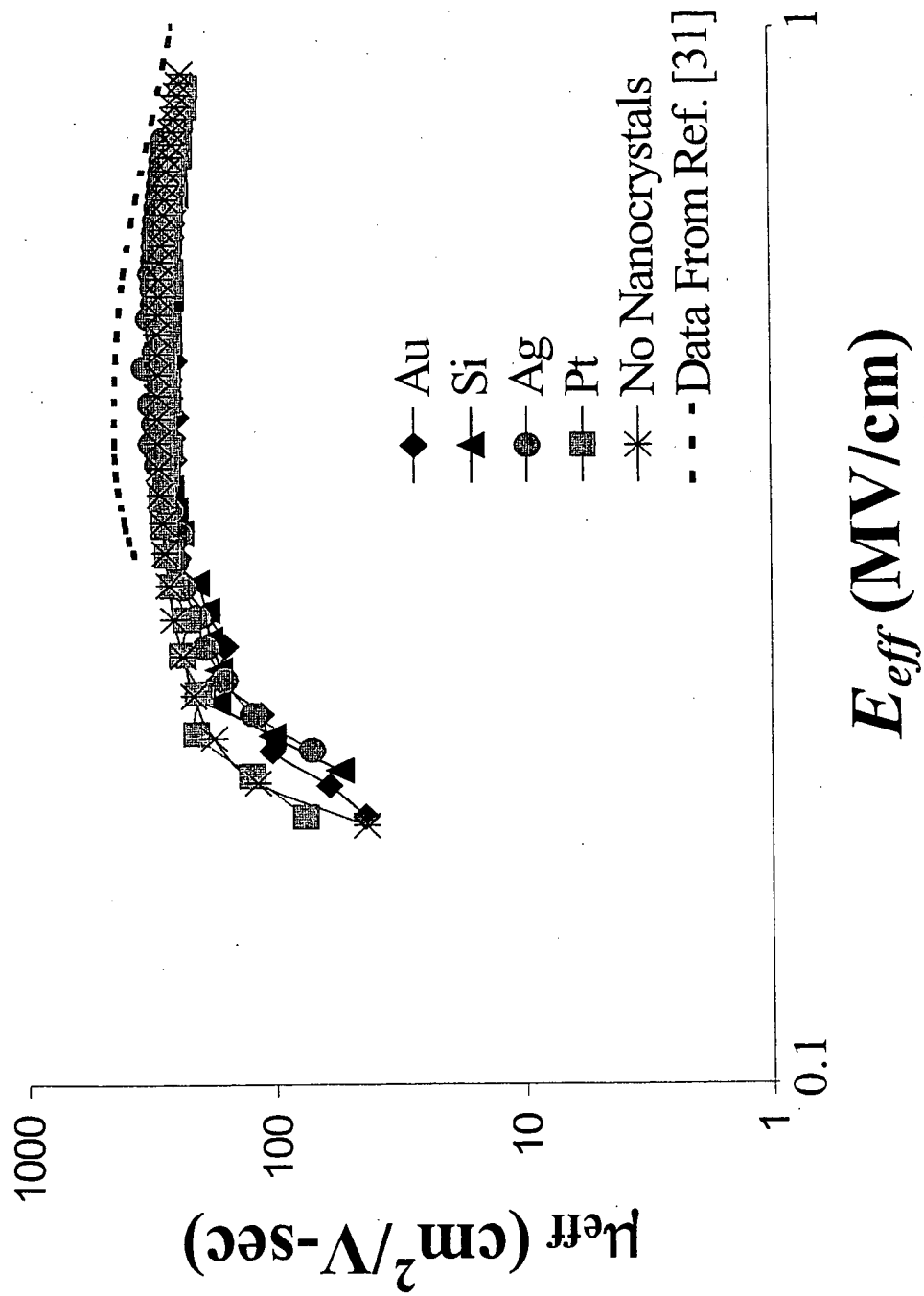
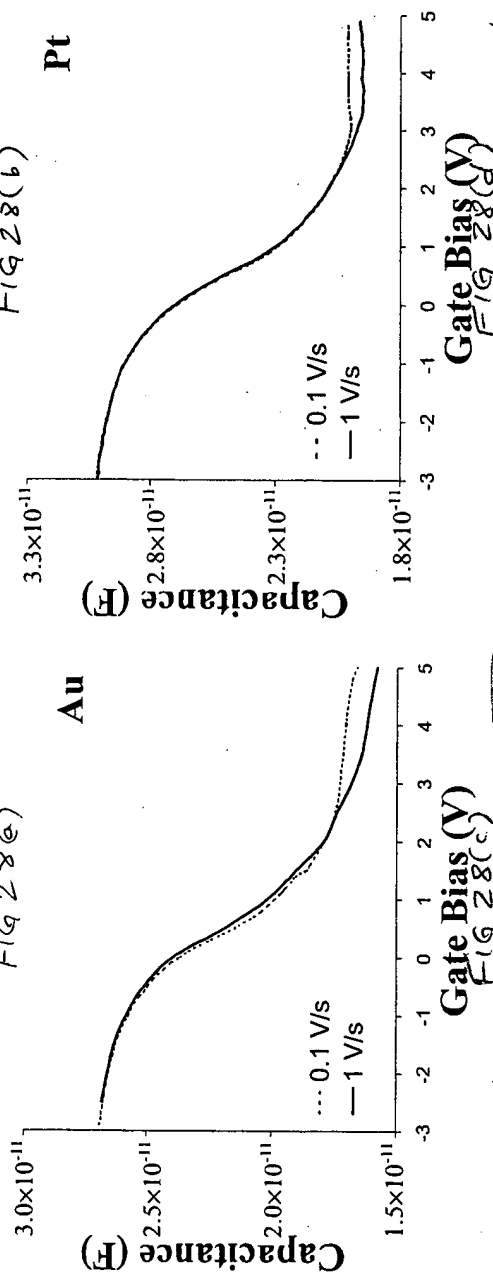
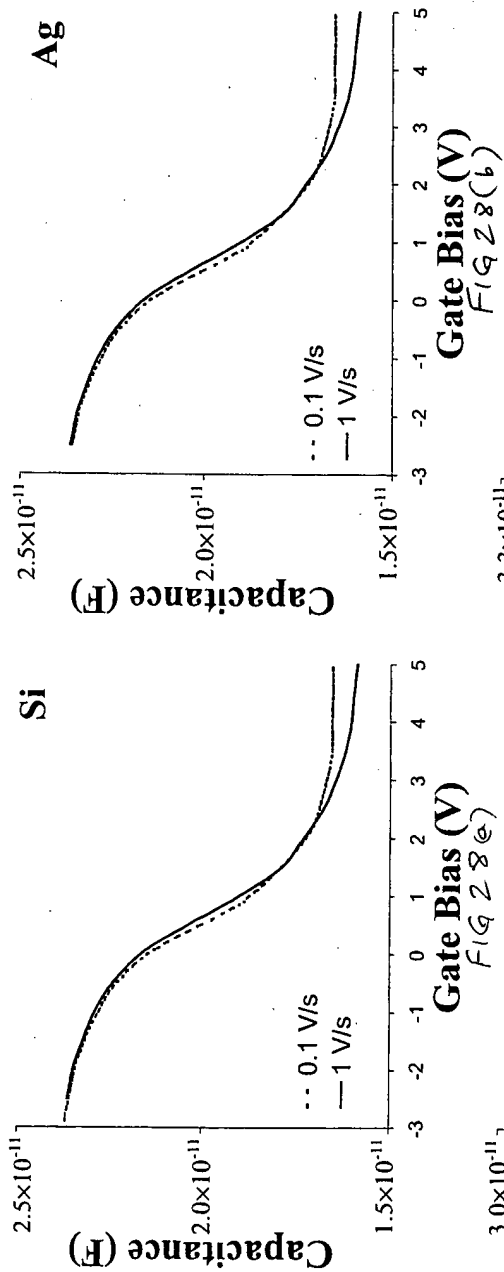


FIG. 27



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